Abstract

A BISR scheme which provides that fuse blocks are shared between memories to reduce hard-BISR implementation costs. The scheme includes a plurality of memories serially connected to a fuse controller. A plurality of fuse blocks are also serially connected to the fuse controller. There are more memory instances than there are fuse blocks, and the fuse controller is configured to allow the fuse blocks to be shared between memories. Preferably, each fuse block includes fuse elements which can be programmed with the memory instance number which needs to be repaired. The fuse block reduces routing congestion and is preferably configured to provide the flexibility of assigning any fuse block to any instance that needs repair. The programmable fuse elements are preferably loaded into a counter (which is preferably part of the fuse controller) which ensures that the correct block information gets loaded into the corresponding memory instance.